REMARKS

The Office Action of 07/20/2006 has been carefully considered. In response thereto, the claims have been amended as set forth above. Reconsideration and allowance in view of the foregoing amendments and the following remarks is respectfully requested.

Independent claims 9 and 14 were rejected as being anticipated by both Goeltzenleuchter and Chennubhotla. The claims have been amended to more clearly distinguish over the cited references, despite the rejections being substantially strained and contrived. Reconsideration is respectfully requested.

Claim 9

In the invention of claim 9, a wrap signal is asserted when a block is accessed non-sequentially by one operation to thereby limit access of another operation to the block. The rejection based on Goeltzenleuchter identifies "means for indicating which buffer is the front buffer" as corresponding to the wrap signal. Claim 9 has therefore been amended to be more express, reciting that wrap signal is asserted *in response to* a condition in which the first buffer operation involves consecutively accessing each buffer location of a block of buffer locations assigned sequential address values in an order different than an order defined by the sequential address values, and is de-asserted *in response to* a condition in which the first buffer operation involves consecutively accessing each buffer location of a block of buffer locations assigned sequential address values in an order the same as an order defined by the sequential address values. No such feature is believed to be taught or suggested by Goeltzenleuchter.

The rejection based on Chennubhotla simply identifies a write enable signal as the "wrap signal." The current amendment is believed to preclude this interpretation.

Claim 14

In the invention of claim 14, a determination is made when the offset address is non-sequential relative to the block address wherein the buffer locations are accessed in an order *different* than an order defined by the sequential address values, and a determinination is made when the offset address is sequential relative to the block address wherein the buffer locations are accessed in an order the *same* as an order defined by the sequential address values. Access of the second buffer operation to locations within the block is *disallowed* when the offset address is non-sequential; and access of the second buffer operation to locations within the block is *allowed* when the offset address is sequential. No such combination of features is believed to be taught or suggested by Goeltzenleuchter.

The rejection based on Chennubhotla simply states that "read or write access to the jitter buffer is always limited to the locations within the buffer." Whereas this interpretation is believed to have gone far beyond the broadest *reasonable* interpretation of claim 14 as previously presented, it is clearly no longer applicable to claim 14 as amended.

Allowance of claims 9-16 is respectfully requested.

Respectfully submitted,

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